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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,606	11/30/2001	Shanjen Pan	TI-31192	4902

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EXAMINER

NGUYEN, CUONG QUANG

ART UNIT	PAPER NUMBER
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2811

NOTIFICATION DATE	DELIVERY MODE
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08/10/2007

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
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Office Action Summary

Application No.

09/998,606

Applicant(s)

PAN ET AL.

Examiner

Cuong Q. Nguyen

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-22 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 18-22 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaartstra (US 6,010,969) in view of Ouellet et al. (US 6,268,620) .

Regarding claim 18, Vaartstra discloses a capacitor structure for a memory device comprising: a semiconductor layer (a semiconductor substrate) having a plurality of recesses formed therein; a dielectric layer (14) formed over the semiconductor layer including within plurality of recesses; and a parallel plate capacitor formed over the dielectric layer, wherein the parallel plate capacitor including a capacitor dielectric (11) of ferroelectric material. See Vaartstra's Fig. 1.

Vaartstra does not teach that the capacitor structure is formed in an analog circuit stage and the parallel plate capacitor extending into and out of plurality of recesses in the semiconductor layer.

Ouellet et al. discloses a capacitor structure could be formed in a memory device or in an analog circuit stage. See Ouellet et al.'s col.1 lines 10-13.

It is noted that Vaartstra's Fig.1 is not drawing into scale. So, the parallel plate capacitor actually may be extending into and out of plurality of recesses in the semiconductor layer. Moreover, the depth of the recesses is considered as an art recognized variable of importance which is subject to routine experimentation and optimization.

It would have been obvious to one of ordinary skill in the art to form Vaartstra's capacitor structure in an analog circuit stage instead of in a memory device because it is known and also taught by Ouellet et al. that the capacitor can be formed in analog circuit stage or in a memory device. It also would have been obvious to one of ordinary skill in the art to the recess deep enough so that the parallel plate capacitor extending into and out of plurality of recesses in the semiconductor layer in order to increase the effective area of the capacitor structure by to routine experimentation and optimization.

Regarding claims 19 and 20, Vaartstra teaches that the capacitor with parallel plates of polysilicon is conventional and well known in the art (col.1, lines 15-20). So, it would have been obvious to one of ordinary skill in the art to form the parallel plate capacitor including first and second polysilicon plates because polysilicon is a common and available material in the art.

Claim 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaartstra in view of Ouellet et al. and further in view of Maniar (US 5,185,689).

Vaartstra and Ouellet et al. teach all the limitations of claims 18 as shown above. These references do not teach that the insulating layer can be formed of PZT or silicon dioxide.

Maniar discloses a capacitor structure comprising: a capacitor insulating layer (22) formed between capacitor plates, wherein the capacitor insulating layer can be silicon dioxide or PZT. See Maniar's Fig.1 and col.3 lines 44-58.

It would have been obvious to one of ordinary skill in the art to form the capacitor insulating layer of PZT or silicon dioxide as taught by Maniar into the device being formed by the combination of Vaartstra and Ouellet et al. because PZT and silicon dioxide are known materials and available in the art.

Response to Arguments

2. Applicant's arguments filed 01-27-04 have been fully considered but they are not persuasive. Applicant argue that Vaartstra does not teach the parallel plate capacitor extend into and out of a plurality of recesses in the semiconductor layer. In response, as above discussed, the depth of the recesses is considered as an art recognized variable of importance which is subject to routine experimentation and optimization. Moreover, the figure in Vaartstra is not in scale, so it would be the insulating layer (14) is thin enough so the parallel plate capacitor could extend into and out of a plurality of recesses in the semiconductor layer. It also would have been obvious to one of ordinary skill in the art to the recess deep enough so that the parallel plate capacitor extending into and out of plurality of recesses in the semiconductor layer in order to increase the effective area of the capacitor structure.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

5. **Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone**

number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.



Cuong Nguyen

Primary examiner

8/5/07